AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method for matching speeds of asynchronous operation between a local chip and a neighboring chip, the method comprising:

deriving an internal frequency signal from an internal oscillator on the local chip;

receiving an external frequency signal from a neighboring chip;

comparing the internal frequency signal with the external frequency signal to generate a control signal;

adjusting the operating speed of the local chip by applying the control signal to the internal oscillator ; and

wherein if the internal frequency signal is faster than the external frequency signal, the control signal causes the internal frequency signal to slow down;

wherein the neighboring chip similarly adjusts the external frequency signal with respect to the internal frequency signal so that the local chip and the neighboring chip operate at a substantially maximum common frequency; and

~~generating a substantially maximum common frequency to be used by the local chip and the neighboring chip by coupling circuitry within the local chip and circuitry within the neighboring chip to generate an asynchronous control loop which generates the substantially maximum common frequency;~~

wherein ~~circuitry in~~ the local chip and ~~circuitry in~~ the neighboring chip are coupled together in ~~to form~~ an asynchronous control loop, which ~~generates a~~ determines the substantially maximum common frequency without reference to an external synchronous clock signal.

2 (Canceled).

3. (Previously presented) The method of claim 1, wherein receiving the external frequency signal from the neighboring chip involves receiving the external frequency signal through a capacitor, an inductor, a resistor, a transmission line, or a direct contact.

4. (Original) The method of claim 1, wherein comparing the internal frequency signal with the external frequency signal involves converting the internal frequency signal and external frequency signal into corresponding current or voltage signals, which are proportional to the frequencies of the frequency signals.

5. (Original) The method of claim 4,

wherein the internal frequency signal and the external frequency signal are converted into corresponding current signals;

wherein comparing the internal frequency signal with the external frequency signal involves comparing the two current signals to generate a difference current signal; and

wherein the method further comprises:

coupling the difference current signal to an integrating capacitor to produce an integrated voltage signal;

applying an offset current source to the integrating capacitor to compensate for transistor leakages, parasitics, and/or nonlinearities; and

coupling the integrating capacitor to an amplifier, wherein the input to the amplifier is the integrated voltage signal and the output of the amplifier is the control signal.

6. (Original) The method of claim 1, further comprising filtering the control signal to improve matching between the local chip's operating speed and the neighboring chip's operating speed.

7. (Original) The method of claim 6, wherein filtering the control signal involves coupling a filter capacitor between the control signal and ground.

8. (Previously presented) The method of claim 1, wherein

the internal frequency signal has a frequency that is a fraction of the internal oscillator frequency of the local chip; and wherein

the external frequency signal has a frequency that is a fraction of an external oscillator frequency of the neighboring chip.

9. (Currently amended) An apparatus for matching speeds of asynchronous operation between a local chip and a neighboring chip, the apparatus comprising:

an internal oscillator on the local chip, from which an internal frequency signal can be derived;

a receiving mechanism configured to receive an external frequency signal from a neighboring chip;

a comparison mechanism configured to compare the internal frequency signal with the external frequency signal to generate a control signal; and

an adjusting mechanism configured to adjust the operating speed of the local chip and the internal oscillator by applying the control signal to the internal oscillator;

wherein if the internal frequency signal is faster than the external frequency signal, the control signal causes the internal frequency signal to slow down;

wherein the neighboring chip similarly adjusts the external frequency signal with respect to the internal frequency signal so that the local chip and the neighboring chip operate at a substantially maximum common frequency; and

~~a generating mechanism configured to generate a substantially maximum common frequency to be used by the local chip and the neighboring chip by coupling circuitry within the local chip and circuitry within the neighboring chip to generate an asynchronous control loop which generates the substantially maximum common frequency;~~

wherein ~~circuitry in~~ the local chip and ~~circuitry in~~ the neighboring chip are coupled together in ~~to form~~ an asynchronous control loop, which ~~generates a~~ determines the substantially maximum common frequency without reference to an external synchronous clock signal.

10 (Canceled).

11. (Original) The apparatus of claim 9, wherein the receiving mechanism is configured to receive the external frequency signal from the neighboring chip through a capacitor, and inductor, a resistor, a transmission line, or a direct contact.

12. (Original) The apparatus of claim 9, wherein the comparison mechanism is configured to convert the internal frequency signal and the external

frequency signal into corresponding current or voltage signals, which are proportional to the frequencies of the frequency signals.

13. (Original) The apparatus of claim 12,

wherein the external frequency signal and the internal frequency signal are converted into corresponding current signals;

wherein the comparison mechanism is configured to compare the two current signals to generate a difference current signal; and

wherein the apparatus further comprises:

an integrating capacitor to which the difference current signal is coupled to produce an integrated voltage signal;

an offset current source applied to the integrating capacitor to compensate for transistor leakages, parasitics, and/or nonlinearities; and

an amplifier to which the integrating capacitor is coupled, wherein the input to the amplifier is the integrated voltage signal and the output of the amplifier is the control signal.

14. (Original) The apparatus of claim 9, further comprising a filtering mechanism configured to filter the control signal to improve matching between the local chip's operating speed and the neighboring chip's operating speed.

15. (Original) The apparatus of claim 14, wherein the filtering mechanism includes a filter capacitor coupled between the control signal and ground.

16. (Previously presented) The apparatus of claim 9, wherein

the internal frequency signal has a frequency that is a fraction of the internal oscillator frequency of the local chip; and wherein

the external frequency signal has a frequency that is a fraction of an external oscillator frequency of the neighboring chip.

17. (Currently amended) A computer system that includes a circuit for matching speeds of asynchronous operation between a local chip and a neighboring chip, the circuit comprising:

a central processing unit;

a semiconductor memory;

an internal oscillator circuit on the local chip, from which an internal frequency signal can be derived;

a receiver circuit for receiving an external frequency signal from a neighboring chip;

a comparison circuit for comparing the internal frequency signal with the external frequency signal to generate a control signal; and

an adjustment circuit for adjusting the operating speed of the local chip and the internal oscillator by applying the control signal to and the internal oscillator;

wherein if the internal frequency signal is faster than the external frequency signal, the control signal causes the internal frequency signal to slow down;

wherein the neighboring chip similarly adjusts the external frequency signal with respect to the internal frequency signal so that the local chip and the neighboring chip operate at a substantially maximum common frequency; and

~~a generator circuit for generating a substantially maximum common frequency to be used by the local chip and the neighboring chip by coupling circuitry within the local chip and circuitry within the neighboring chip to generate an asynchronous control loop which generates the substantially maximum common frequency;~~

wherein ~~circuitry in~~ the local chip and ~~circuitry in~~ the neighboring chip are coupled together in ~~to form~~ an asynchronous control loop, which ~~generates a~~ determines the substantially maximum common frequency without reference to an external synchronous clock signal.

18 (Canceled).

19. (Original) The computer system of claim 17, wherein the receiver circuit is configured to receive the external frequency signal from the neighboring chip through a capacitor, and inductor, a resistor, a transmission line, or a direct contact.

20. (Original) The computer system of claim 17, wherein the comparison circuit is configured to convert the internal frequency signal and the external frequency signal into corresponding current or voltage signals, which are proportional to the frequencies of the frequency signals.

21. (Original) The computer system of claim 20,

wherein the external frequency signal and the internal frequency signal are converted into corresponding current signals;

wherein the comparison circuit is configured to compare the two current signals to generate a difference current signal; and

wherein the computer system further comprises:

an integrating capacitor to which the difference current signal is coupled to produce an integral voltage signal;

an offset current source applied to the integrating capacitor to compensate for transistor leakages, parasitics, and/or nonlinearities; and

an amplifier to which the integrating capacitor is coupled, wherein the input to the amplifier is the integral voltage signal and the output of the amplifier is the control signal.

22. (Original) The computer system of claim 17, further comprising a filtering circuit for filtering the control signal to improve matching between the local chip's operating speed and the neighboring chip's operating speed.

23. (Original) The computer system of claim 22, wherein the filter circuit includes a filter capacitor coupled between the control signal and ground.

24. (Previously presented) The computer system of claim 17, wherein the internal frequency signal has a frequency that is a fraction of the internal oscillator frequency of the local chip; and wherein the external frequency signal has a frequency that is a fraction of an external oscillator frequency of the neighboring chip.

25. (Previously presented) The method of claim 1, wherein adjusting the frequency of the local chip involves changing the power-supply voltage of the local chip.

26. (Previously presented) The apparatus of claim 9, wherein the adjusting mechanism is configured to adjust the frequency of the local chip by changing the power-supply voltage of the local chip.

27. (Previously presented) the computer system of claim 17, wherein the adjustment circuit is configured to adjust the frequency of the local chip by changing the power-supply voltage of the local chip.